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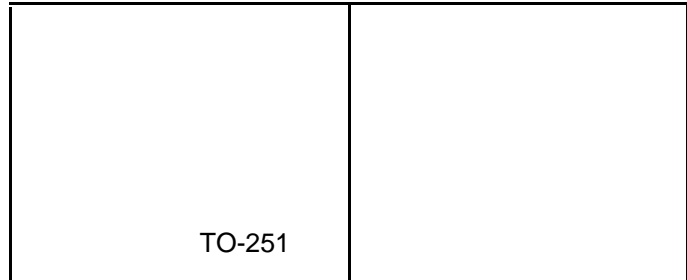
MPSU70M1K5

Power MOSFET

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Features

- z $BV_{DSS}=700\text{ V}$, $I_D=3\text{ A}$
- z $R_{DS(on)}:1.5\ \Omega$ (Max) ! $V_{GS}=10\text{V}$
- Very Low FOM ($R_{DS(on)} \times Q_g$)
- 100% Avalanche Tested
- RoHS compliant



Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

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Absolute Maximum Ratings T_J=25°C unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	700	V
V_{GS}	Gate-Source Voltage	±20	V
$I_D^{(1)}$	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	3.0	A
	Drain Current - Continuous ($T_C = 100^\circ\text{C}$)	1.9	A
$I_{DM}^{(2)}$	Drain Current - Pulsed	8.4	A
$E_{AS}^{(3)}$	Single Pulsed Avalanche Energy	43	mJ
I_{AR}	Avalanche Current	1	A
dv/dt	MOSFET dv/dt ruggedness, $V_{DS}=0\dots560\text{V}$	50	V/ns
dv/dt	Reverse diode dv/dt, $V_{DS}=0\dots560\text{V}$, $I_{DS}\leq I_D$	15	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	49	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2500	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	-	2.54	°C/W
$R_{\theta JA}$	Junction-to-Ambient	-	62.5	°C/W



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Electrical Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
On Characteristics						
V _{GS}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 60 μA	2.5	-	3.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 1.1 A	-	1.35	1.5	Ω
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	700	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 700 V, V _{GS} = 0 V, T _C = 25°C	-	-	1	μA
		V _{DS} = 700 V, V _{GS} = 0 V, T _C = 150°C	-	-	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1.0 MHz	-	245	-	pF
C _{oss}	Output Capacitance		-	13	-	pF
C _{riss}	Reverse Transfer Capacitance		-	1.7	-	pF
Switching Characteristics						
t _{d(on)}	Turn-On Time	V _{DS} = 350 V, I _D = 1.5 A, R _G = 25 Ω (Note 4,5)	-	20	-	ns
t _r	Turn-On Rise Time		-	18	-	ns
t _{d(off)}	Turn-Off Delay Time		-	50	-	ns
t _f	Turn-Off Fall Time		-	20	-	ns
Q _g	Total Gate Charge	V _{DS} = 560 V, I _D = 1.5 A, V _{GS} = 10 V (Note 4,5)	-	5.5	-	nC
Q _{gs}	Gate-Source Charge		-	1.1	-	nC
Q _{gd}	Gate-Drain Charge		-	2.2	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	3.0	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	8.4	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 3.0 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 1.5 A	-	135	-	ns
Q _{rr}	Reverse Recovery Charge	di _F /dt = 100 A/μs	-	0.6	-	μC

Notes :

- Limited by T_J max. Maximum duty cycle D=0.50
- Repetitive Rating : Pulse width limited by maximum junction temperature
- I_{AS}=1A, V_{DD}=50V, R_G=25Ω, Starting T_J =25°C
- Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
- Essentially Independent of Operating Temperature



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Figure 1. On Region Characteristics

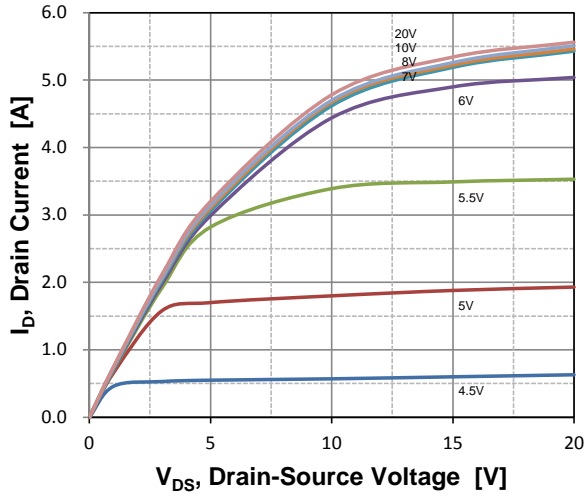


Figure 2. Transfer Characteristics

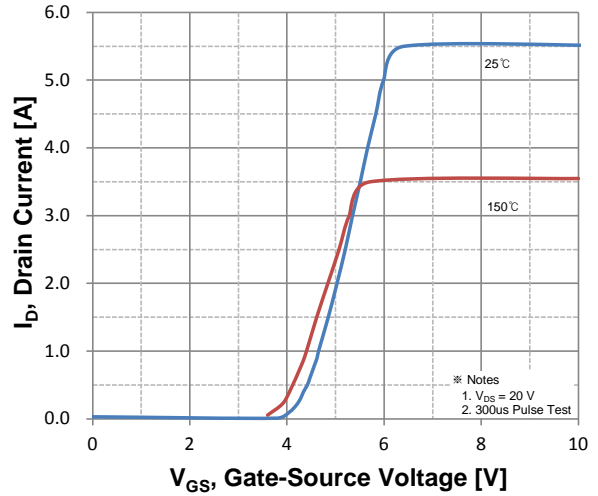


Figure 3. On Resistance Variation vs. Drain Current and Gate Voltage

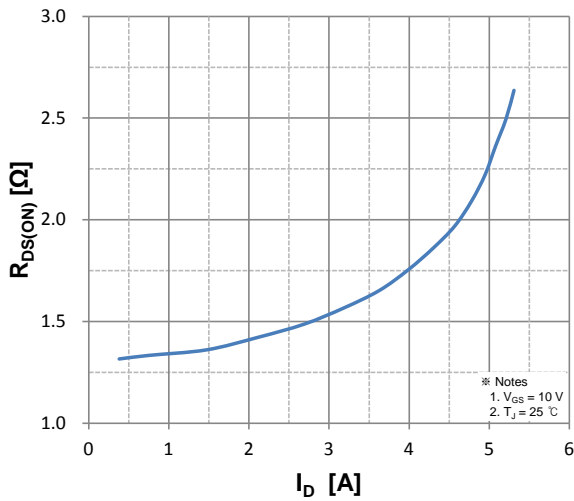


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

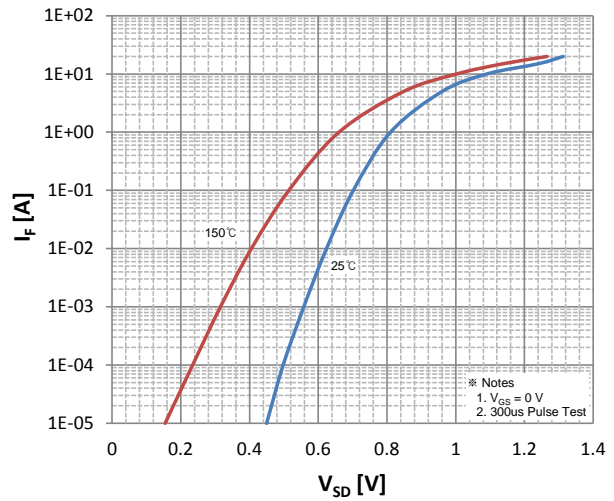


Figure 5. Capacitance Characteristics

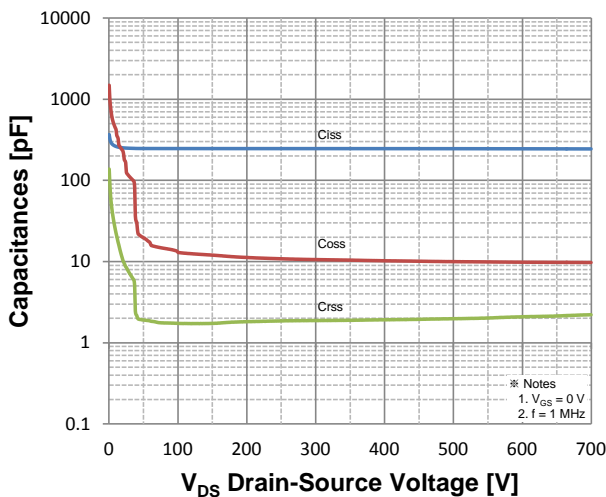
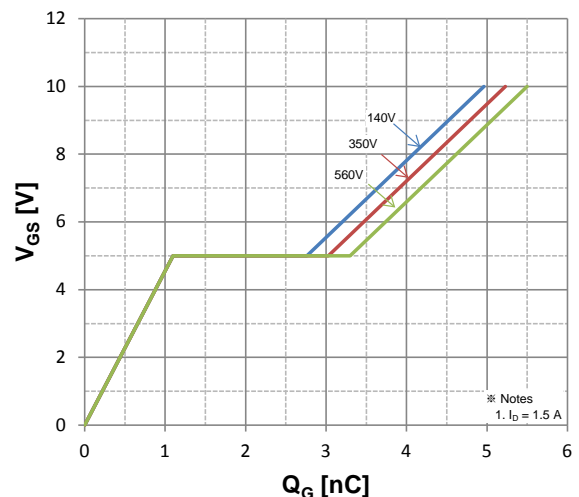


Figure 6. Gate Charge Characteristics





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Figure 7. Breakdown Voltage Variation vs. Temperature

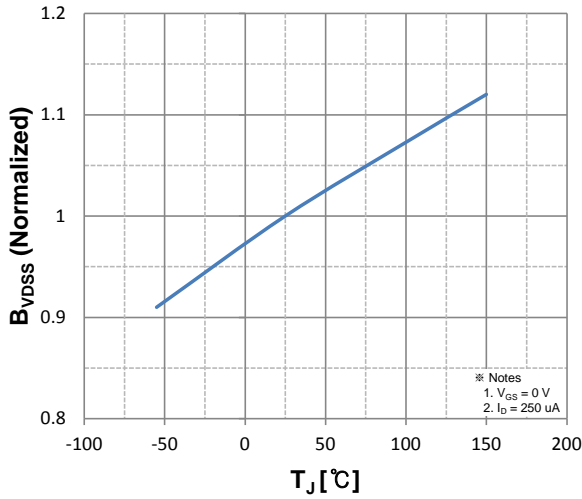


Figure 8. On-Resistance Variation vs. Temperature

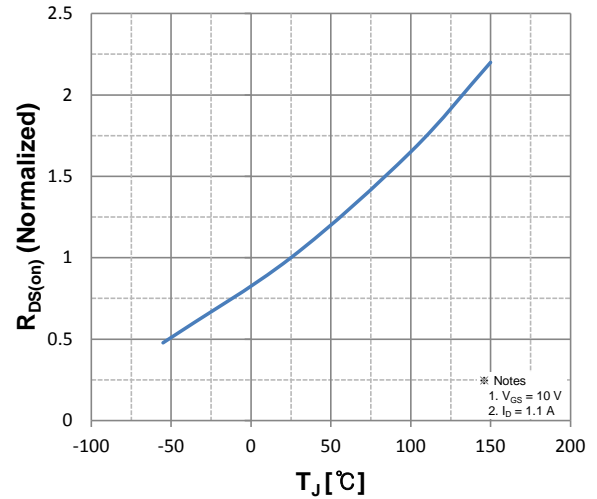


Figure 9. Maximum Safe Operating Area

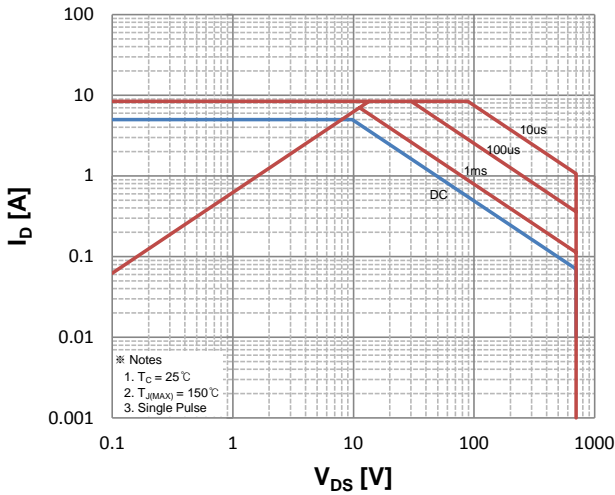


Figure 10. Maximum Drain Current vs. Temperature

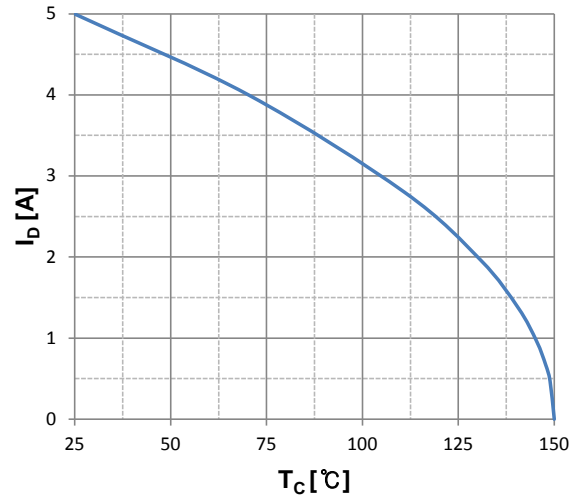


Figure 11. Transient Thermal Response Curve

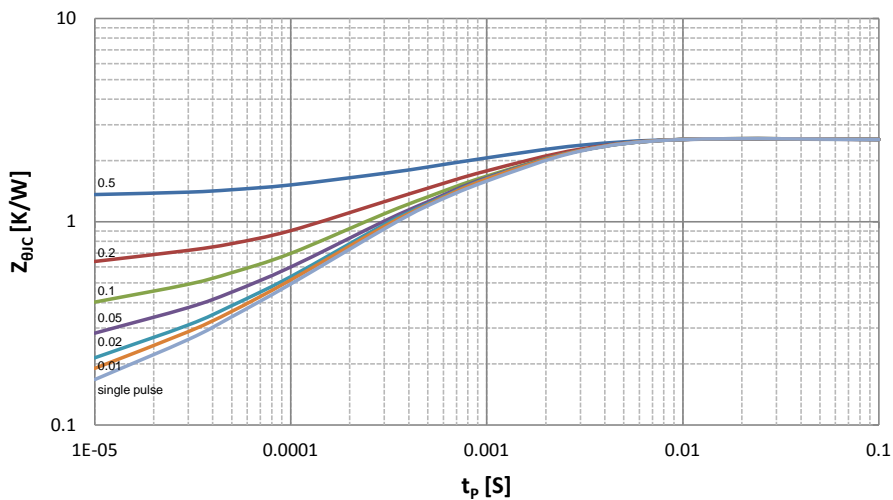


Figure 12. Gate Charge Test Circuit and Waveform

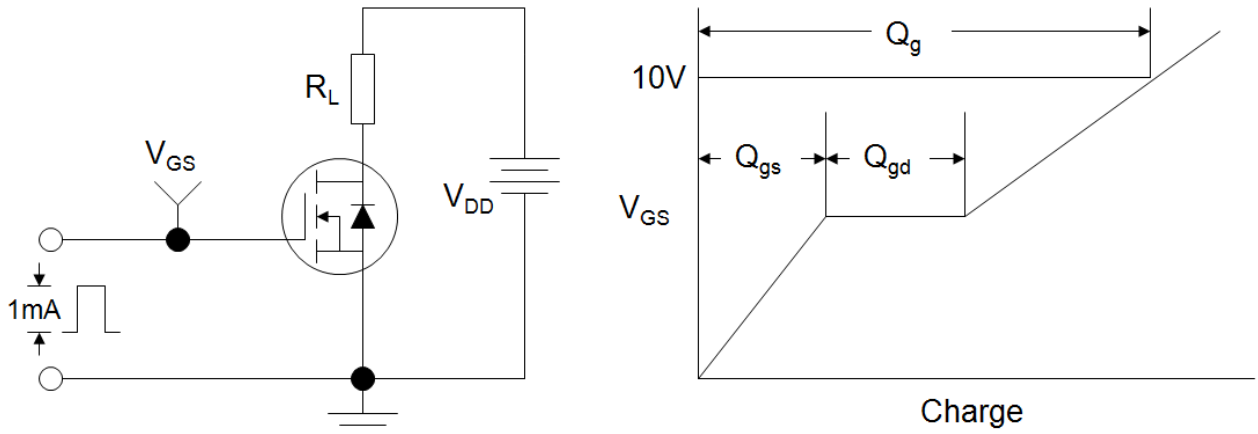


Figure 13. Resistive Switching Test Circuit and Waveform

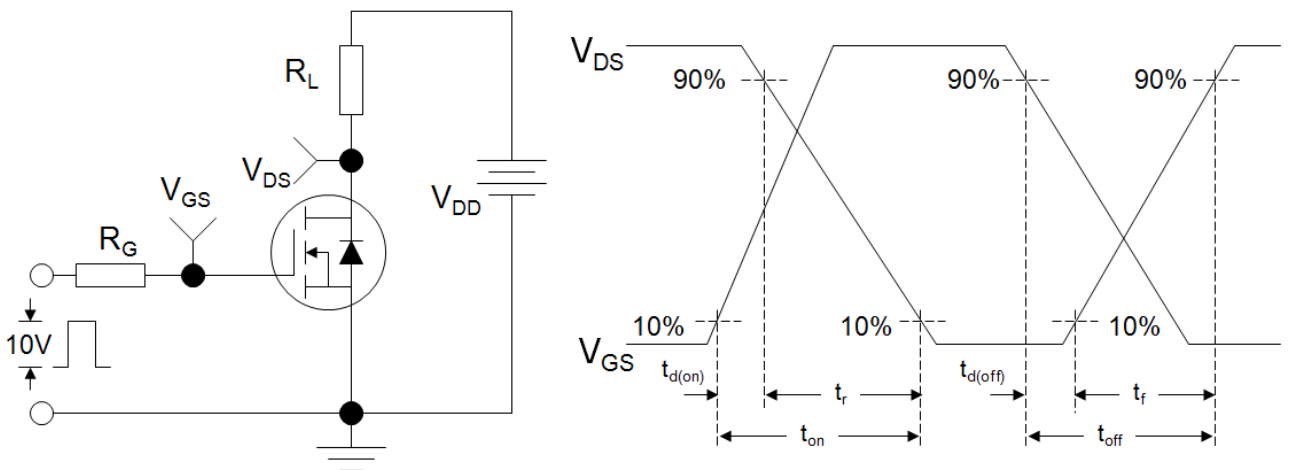
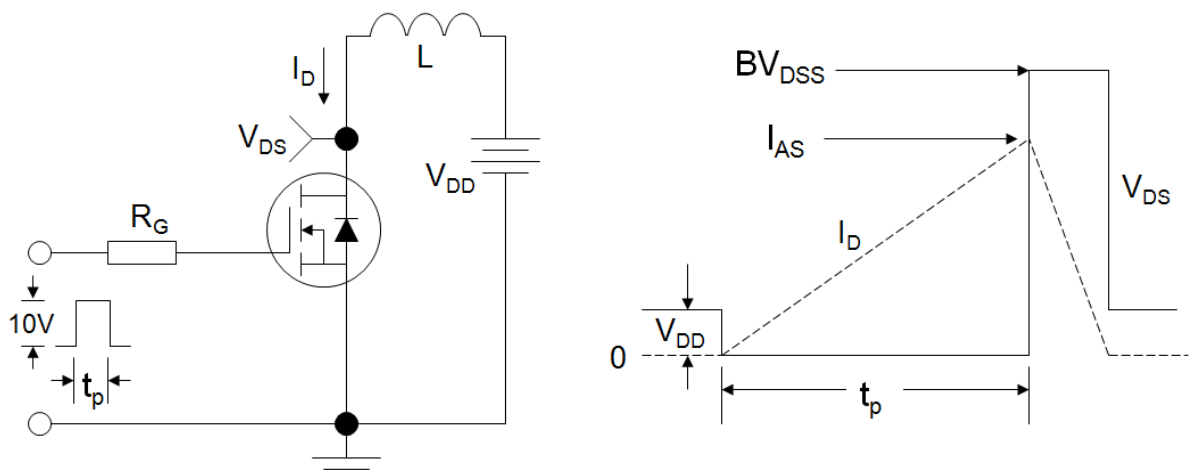


Figure 14. Unclamped Inductive Switching Test Circuit and Waveform





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